OF ECS-01-132

December 12, 2003

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/664,211 09/17/03

Purakh Raj Verma et al.

A METHOD OF MAKING DIRECT CONTACT ON GATE BY USING DIELECTRIC STOP LAYER

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December (9, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

- U.S. Patent 5,731,239 to Wong et al., "Method of Making Self-Aligned Silicide Narrow Gate Electrodes for Field Effect Transistors Having Low Sheet Resistance," describes a method for making low sheet resistance sub quarter micrometer gate electrode in FET devices.
- U.S. Patent 6,010,954 to Ho et al., "CMOS Gate Architecture for Integration of Salicide Process in Sub 0.1uM Devices," describes a method to form a "mushroom shaped" gate structure that increases the top gate silicide contact area and improves the salicidation process.
- U.S. Patent 6,271,087 to Kinoshita et al., "Method for Forming Self-Aligned Contacts and Local Interconnects Using Self-Aligned Local Interconnects," describes a method for forming self-aligned contacts and local interconnects.
- U.S. Patent 6,281,059 to Cheng et al., "Method of Doing ESD Protective Device Ion Implant Without Additional Photo Mask," describes a method of forming ESD protective transistor.

Sincerely

Stephen B. Ackerman, Reg. No. 37761

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citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.